UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,064	10/10/2001	Ishai Nachumovsky	TSL-040	1015

22888 7590 01/28/2004

BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,064	NACHUMOVSKY, ISHAI	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/10/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-17,23-25 and 29-43* is/are rejected.

7)☒ Claim(s) *6-9,18-22 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/10/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 10-17, 23-25, 29-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yojima et al. (6,133,744 and Yojima hereinafter).

Claims 1 and 23-25:

Yojima teaches the invention substantially as claimed. Yojima teaches (figure 2) an apparatus (21) includes multiplayered substrate (22) and a contact film (24). The plurality of LSI test chips (23) mounted on an upper surface of the substrate (22) and functioning as a semiconductor wafer tester, and the contact film (24) having a first set of bumps (25a) formed on an upper surface of the contact film (24) and a second set of bumps (25b) formed on a lower surface of the contact film (24). The contact film (24) is sandwiched between the multi-layered substrate (22) and a semiconductor wafer (29) to be tested so that the first set of bumps are in electrical contact with the contact of the substrate (22) and the second set of bumps are in electrical contact with the semiconductor wafer (figure 2 column 4 lines 15-36).

Yojima does not explicitly teach the auxiliary test circuit. Yojima, however, teaches that the LSI test chips (23) are electrically connected to contacts formed on a lower surface of the substrate (22) through internal wirings (26) (column 4 lines 21-24).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to name Yojima's LSI test chips (23) as "auxiliary test circuit". One having ordinary skill in the art would be motivated to do so because naming Yojima's LSI chips as "auxiliary test circuit" would not affect LSI chips' performance nor LSI chips' connection of the LSI chips (23) to be contacted to the lower surface of the substrate (22) (column 4 lines 21-24).

Claims 2-3:

Yojima further teaches that an external tester (32) provides electric power to the apparatus (21) and transmits signals to and receives signals from the apparatus (32) through I/O pins thereof (column 4 lines 41-45).

Claim 4:

Yojima teaches the testing of a DRAM semiconductor wafer (column 1 lines 11-12). Yojima also teaches that fail memory data are transmitted to the external tester (32) after receiving response output signals transmitted from the semiconductor chips mounted on the wafer (29) to be tested (column 4 lines 59-65).

Claim 5:

Yojima teaches plurality of LSI test chips (23) (figure 2).

Claims 10-12 and 16-17:

Yojima's apparatus including a contact film having at least one first bump formed on an upper surface thereof and at least one second bump formed on a lower surface thereof. The first bump is electrically connected to the second bump through an internal wiring formed throughout the contact film, and at least a part of the internal wiring and the first and the second bumps is made of shape memory alloy. The contact film is to be disposed to be sandwich between the substrate and a semiconductor wafer to be tested so that the first bump is in electrical contact with the contact of the substrate and the second bump is in electrical contact with the semiconductor wafer (column 3 lines 6-23).

Claim 13-15:

Yojima's LSI test chips (23) have various functions of an LSI tester such as a pin electronics card including a driver and a comparator, a pattern memory, a formatter circuit, a dock generating circuit and a DC or AC measuring circuit. In addition, Yojima's external tester (32) transmits test data such as test patterns, waveform formats and timing data to the LSI test chips (23), the concurrently the LSI test chips (23) apply signals to a plurality of semiconductor chips mounted on the wafer (29) to be tested. Response output signals transmitted from the semiconductor chip mounted on the wafer (29) are received by the LSI test chips (23). The thus received response signals are compared with an expected value in the LSI test chip (column 4 lines 45-65).

Claim 29:

Yojima teaches the invention substantially as claimed. Yojima teaches (figure 2) an apparatus (21) includes multiplayered substrate (22) and a contact film (24). The plurality of LSI test chips (23) mounted on an upper surface of the substrate (22) and functioning as a semiconductor wafer tester, and the contact film (24) having a first set of bumps (25a) formed on an upper surface of the contact film (24) and a second set of bumps (25b) formed on a lower surface of the contact film (24). The contact film (24) is sandwiched between the multi-layered substrate (22) and a semiconductor wafer (29) to be tested so that the first set of bumps are in electrical contact with the contact of the substrate (22) and the second set of bumps are in electrical contact with the semiconductor wafer (figure 2 column 4 lines 15-36).

Yojima does not explicitly teach a plurality of traces coupling the first set of pads to the second set of pads. Yojima, however, teaches the internal wiring (26) and the internal wiring (27) are electrically connected to each of the first set of bumps (26a) and the second set of bumps (25b), respectively (figure 2, column 4 lines 15-29).
It would have been obvious to one skilled in the art at the time the invention was made to name Yojima's wirings (26 & 27) as "plurality of traces". One having ordinary skill in the art would be motivated to do so because naming Yojima's wirings as "plurality of traces" would not affect Yojima's wirings' connections.

Claims 30-32 and 36-38 and 39:

Claims 30, (31 & 32), 36, 37, 38 and (39-41) are rejected for reasons similar to those set forth against claims 11, 12, 13, 14, 15 and 16, respectively.

Claims 33-35:

Yojima teaches that the LSI chips (23) includes a pattern memory which receives test patterns, waveform formats and timing data to be apply to plurality of semiconductor chips. The LSI chips (23) also includes comparator (column 4 lines 45-65).

Claim 42:

Yojima shows the wirings (26) are connected to the LSI test chips (23) (figure 2).

Claim 43:

Yojima's LSI chips (23) have various functions of an LSI tester such as a pin electronic card including a driver, a comparator, a pattern memory, a formatter circuit, a dock generating circuit and a DC and AC measuring circuit (column 4 lines 44-49).

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703)746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Christine T. Tu
Primary Examiner
Art Unit 2133

January 20, 2004